CLAIMS

1. A control system, comprising:

a data circuit configured to communicate computer readable data with a component via a data transfer bus;

a control circuit configured to control a frequency spread deviation for data communication via the data transfer bus;

a data register configured to maintain an operating conditions status of the data circuit, the operating conditions status corresponding to data communications loading on the data transfer bus;

control logic configured to:

obtain the operating conditions status from the data register; and

generate a control circuit input to adjust the frequency spread deviation according to the operating conditions status.

2. A control system as recited in claim 1, wherein the control circuit is a phase-locked loop configured to receive the control circuit input and adjust the frequency spread deviation.

3. A control system as recited in claim 1, wherein operating conditions of the data circuit include at least one of a process, a voltage, and a temperature operating condition.

4. A control system as recited in claim 1, wherein the control circuit is further configured to control the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for data communication.

5. A control system as recited in claim 1, wherein the control circuit is further configured to control the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for data communication.

6. A control system as recited in claim 1, further comprising an application specific integrated circuit (ASIC) that includes the data circuit, the control circuit, and the data register.

7. A control system as recited in claim 6, wherein:

the component is a memory component;

the data transfer bus is a memory bus; and

the data circuit is further configured to communicate the computer readable data to the memory component via the memory bus.

8. A control system as recited in claim 6, wherein the ASIC further includes variable connection drive pads, and wherein operating conditions of the ASIC include process, voltage, and temperature operating conditions.

9. A control system as recited in claim 6, wherein the ASIC further includes variable connection drive pads, and wherein operating conditions of the ASIC vary according to a drive current strength of a variable connection drive pad.

10. A control system as recited in claim 1, wherein the control logic is implemented as firmware in the control system.

11. A control system as recited in claim 1, wherein the control logic is further configured to generate the control circuit input to adjust the frequency spread deviation to minimize electromagnetic emissions associated with data communication via the data transfer bus.

12. A data transfer circuit configured to adjust a frequency spread deviation for spread spectrum clocking of a data transfer via a data transfer bus according to operating conditions of the data transfer circuit, the operating conditions corresponding to data transfer bus loading.

13. A data transfer circuit as recited in claim 12, wherein the operating conditions of the data transfer circuit include at least one of a process, a voltage, and a temperature operating condition.

14. A data transfer circuit as recited in claim 12, wherein the data transfer circuit is further configured to control the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for the data transfer.

15. A data transfer circuit as recited in claim 12, wherein the data transfer circuit is further configured to control the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for the data transfer.

16. A data transfer circuit as recited in claim 12, wherein the data transfer circuit is further configured to obtain an operating conditions status from a data register, and wherein the data transfer circuit is further configured to adjust the frequency spread deviation according to the operating conditions status.

17. A data transfer circuit as recited in claim 12, wherein the data transfer circuit is further configured to obtain an operating conditions status from a data register, the operating conditions status corresponding to process, voltage, and temperature operating conditions of the data transfer circuit.

18. A data transfer circuit as recited in claim 12, wherein the data transfer circuit includes variable connection drive pads to couple the data transfer bus, and wherein the data transfer circuit is further configured to obtain an operating conditions status from a data register, the operating conditions status varying according to a drive current strength of a variable connection drive pad.

19. A data transfer circuit as recited in claim 12, wherein the data transfer circuit is further configured to adjust the frequency spread deviation to minimize electromagnetic emissions associated with the data transfer via the data transfer bus.

20. A data transfer circuit as recited in claim 12, wherein the data bus is expandable for variable data transfer, and wherein the data transfer circuit is further configured to adjust the frequency spread deviation to minimize electromagnetic emissions associated with the variable data transfer via the data transfer bus.

21. A control system, comprising an application specific integrated circuit (ASIC) and control logic, wherein:

the ASIC is configured to transfer data to a memory component via a memory bus, the ASIC including:

a clocking control configured to control a frequency spread deviation for data transfer via the memory bus; and

a process-voltage-temperature (PVT) status register configured to maintain a PVT status of the ASIC, the PVT status corresponding to memory bus loading;

the control logic is configured to:

obtain the PVT status from the PVT register; and

generate a clocking control input to adjust the frequency spread deviation according to the PVT status.

22. A control system as recited in claim 21, wherein the clocking control is a phase-locked loop configured to receive the clocking control input and adjust the frequency spread deviation.

23. A control system as recited in claim 21, wherein the clocking control is further configured to control the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for data transfer.

24. A control system as recited in claim 21, wherein the clocking control is further configured to control the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for data transfer.

25. A control system as recited in claim 21, wherein the ASIC further *includes variable connection drive pads, and wherein* PVT *operating conditions* of the ASIC vary according to a drive current strength of a variable connection drive pad.

26. A control system as recited in claim 21, wherein the control logic is implemented as firmware in the control system.

27. A control system as recited in claim 21, wherein the control logic is further configured to generate the clocking control input to adjust the frequency spread deviation to minimize electromagnetic emissions associated with data transfer via the memory bus.

28. A method, comprising:

controlling a frequency spread deviation for data transfer to a component via a data transfer bus;

maintaining an operating conditions status that corresponds to data transfer loading on the data transfer bus; and

generating an input to adjust the frequency spread deviation according to the operating conditions status.

29. A method as recited in claim 28, further comprising obtaining the operating conditions status from a data register.

30. A method as recited in claim 28, further comprising:

obtaining the operating conditions status from a data register; and

setting a drive current strength of a variable connection drive pad according to the operating conditions status.

31. A method as recited in claim 28, further comprising adjusting the frequency spread deviation to minimize electromagnetic emissions associated with data transfer via the data transfer bus.

32. A method as recited in claim 28, wherein controlling includes controlling the frequency spread deviation with a phase-locked loop configured to receive the input to adjust the frequency spread deviation.

33. A method as recited in claim 28, wherein controlling includes controlling the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for the data transfer.

34. A method as recited in claim 28, wherein controlling includes controlling the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for the data transfer.

35. A method as recited in claim 28, wherein the operating conditions status corresponds to at least one of a process, a voltage, and a temperature operating condition.

36. A method, comprising:

controlling a frequency spread deviation for data communication with a memory component via a memory bus;

maintaining a process-voltage-temperature (PVT) status that corresponds to data loading on the memory bus, the PVT status indicating operating conditions of an application specific integrated circuit (ASIC); and

generating an ASIC input to adjust the frequency spread deviation according to the PVT status.

37. A method as recited in claim 36, further comprising obtaining the PVT status from a PVT data register.

38. A method as recited in claim 36, further comprising:

obtaining the PVT status from a PVT data register; and

setting a drive current strength of a variable connection drive pad of the ASIC according to the PVT status.

39. A method as recited in claim 36, further comprising adjusting the frequency spread deviation to minimize electromagnetic emissions associated with data communication via the memory bus.

40. A method as recited in claim 36, wherein controlling includes controlling the frequency spread deviation with a phase-locked loop, the phase-locked loop configured to receive the ASIC input to adjust the frequency spread deviation.

41. A method as recited in claim 36, wherein controlling includes controlling the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for the data communication.

42. A method as recited in claim 36, wherein controlling includes controlling the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for the data communication.

43. One or more computer-readable media comprising computer executable instructions that, when executed, direct a printing device to:

control a frequency spread deviation for data transfer to a memory component via a memory bus;

maintain a process-voltage-temperature (PVT) status that corresponds to data transfer loading on the memory bus, the PVT status indicating operating conditions of an application specific integrated circuit (ASIC); and

generate an ASIC input to adjust the frequency spread deviation according to the PVT status.

44. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to obtain the PVT status from a PVT data register.

45. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to:

obtain the PVT status from a PVT data register; and

set a drive current strength of a variable connection drive pad of the ASIC according to the PVT status.

46. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to adjust the frequency spread deviation to minimize electromagnetic emissions associated with data transfer via the memory bus.

47. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to control the frequency spread deviation with a phase-locked loop, the phase-locked loop configured to receive the ASIC input to adjust the frequency spread deviation.

48. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to control the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for data transfer.

49. One or more computer-readable media as recited in claim 43, further comprising computer executable instructions that, when executed, direct the printing device to control the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for the data transfer.

50. A data transfer system, comprising:

means to control a frequency spread deviation for data transfer via a data transfer bus;

means to obtain an operating conditions status that corresponds to data transfer loading on the data transfer bus; and

means to generate an input to adjust the frequency spread deviation according to the operating conditions status.

51. A data transfer system as recited in claim 50, further comprising means to maintain the operating conditions status.

52. A data transfer system as recited in claim 50, further comprising means to adjust a drive current strength of a variable connection drive pad according to the operating conditions status.

53. A data transfer system as recited in claim 50, further comprising means to adjust the frequency spread deviation to minimize electromagnetic emissions associated with data transfer via the data transfer bus.